SANJAY KUMAR

Senior Software Architect | SoC Virtual Platforms & Hybrid Emulation | GenAI for EDA

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Bengaluru, Karnataka, India | CV: https://yajnas07.github.io/cv

PROFESSIONAL SUMMARY

Senior Software Architect with 22+ years of experience designing complex hardware–software hybrid systems at the intersection of virtual platforms, silicon bring-up, and enterprise engineering. Expert in SystemC/TLM 2.0 methodology, AMBA bus modeling, and hybrid emulation infrastructure. Leads teams to deliver SoC virtual platforms that compress hardware development cycles and enable pre-silicon software bring-up. Deeply invested in applying Generative AI and LLM-powered tooling to transform EDA workflows. Holds B.Tech (CS) from NIT Trichy and M.S. (Microelectronics) from BITS Pilani.

TECHNICAL SKILLS

Core Domain: SystemC / TLM 2.0, Virtual Platform Integration, Hybrid Emulation, IP Modeling, SoC Architecture

Bus & Protocol: AMBA AXI / CHI / AMBA-PV, DDR4/5, LPDDR4/5, UFS, NVMe, USB, Ethernet, CSI-2, DSI, HDMI, I2C

Architecture: ARM RME / GPC / GPT, AArch64, NoC, Memory Controllers, TrustZone

Languages: C++17/20, SystemC, Python, TCL, JavaScript, HTML/CSS

Tools & Infra: Git / GitHub, Linux, Make / CMake, VS Code (Remote SSH), SystemC Catalog Browser

AI / GenAI: LLM-assisted development (Claude Code), Prompt Engineering, RAG Pipelines, Agentic AI, Manim Animations

Soft Skills: Technical Leadership, Customer Engagement, Cross-functional Collaboration, Mentoring

PROFESSIONAL EXPERIENCE

Senior Software Architect — Cadence Design Systems

Jul 2024 – Present (1 yr 11 mo) | Bengaluru, India

- Deployed hybrid emulation solutions at tier-1 SoC customers, enabling full OS boot (Linux and Android) on virtual and hybrid platforms.
- Owned full-stack delivery: virtual IP modeling, HW/SW transactor development, hybrid platform integration, and embedded SW bring-up.
- Pioneering a multi-threaded simulation framework addressing SystemC's longstanding single-thread architectural limitation — targeting significant improvement in simulation throughput for complex SoC designs.
- Driving adoption of GenAI-assisted development workflows; used Claude Code agent mode to build a Virtio P9 model in ~1 week vs. a traditional 2–3 month timeline.

Software Architect — Cadence Design Systems

Oct 2020 – Jul 2024 (3 yr 10 mo) | Bengaluru, India

- Led end-to-end delivery of the Helium Virtual and Hybrid Platform Catalog: UFS, NVMe, Ethernet, USB IP models; AMBA bus transactors; bare-metal, Linux, and Android SW stacks.
- Designed a virtual-to-RTL gear-shift execution platform enabling seamless architectural state transfer from virtual CPUs to RTL CPUs for silicon-representative benchmarking.
- Enabled pre-silicon software development for mobile and hyperscaler SoC customers, compressing time-to-market by allowing SW development months ahead of first silicon.
- Built VS Code extension for a SystemC catalog browser (tree-view, build status, doc preview, terminal integration) running over SSH on remote Linux filesystems.

Senior Principal Software Engineer — Cadence Design Systems

Jul 2016 – Oct 2020 (4 yr 4 mo) | Bengaluru, India

- Architected Cadence Smart Memory — a high-performance coherent memory solution that significantly accelerated hybrid RTL + SystemC platform execution.
- Built a comprehensive virtual device model library: CSI-2 Camera, DSI Display, HDMI, and I2C, enabling realistic pre-silicon validation across imaging and display subsystems.

Principal Solutions Engineer — Cadence Design Systems

Mar 2014 – Jul 2016 (2 yr 5 mo) | Bengaluru, India

- Led hybrid platform integration and full-stack SW bring-up (bare-metal through OS) for multiple ARMv8-based mobile SoC programs at in-house and customer sites.

Technical Lead — Texas Instruments

Feb 2012 – Mar 2014 (2 yr 2 mo) | Bengaluru, India

- Led end-to-end execution of IVAHD 2.0 Virtual Platform — one of the industry's pioneering SystemC adoption projects at TI.

- Drove TI's strategic transition from proprietary SSI-based modeling to OSCI SystemC, establishing the foundational architecture for all subsequent TI VP initiatives.
- Solved first-of-its-kind SystemC integration challenges (runtime pin binding, synchronization, reset handling); solutions became reference implementations for the VP community.
- Developed SystemC Reset Infrastructure using SC 2.3 process-control APIs; presented at ISCUG 2013 to industry recognition.

Sr. Software Engineer — Texas Instruments

Aug 2007 – Jan 2012 (4 yr 6 mo) | Bengaluru, India

- Developed cycle-accurate models for TI Curie-class SoCs achieving >95% cycle accuracy using event-based simulation techniques.
- Built detailed models for TI CBA subsystem: SCR, M2M Bridge, VBSUM/VBUSP bus infrastructure.
- Conceptualized debug infrastructure for Data Breakpoint and UMR detection, significantly improving model debugging efficiency.

Software Engineer — Texas Instruments

Oct 2005 – Jul 2007 (1 yr 10 mo) | Bengaluru, India

- Developed Simulation Toolkit and connection drivers based on TI's proprietary SSI modeling standard.
- Built code generators using scripting languages to automatically produce C++ model scaffolding from structured input descriptions.

Software Engineer — Siemens Information Systems Ltd

Jul 2004 – Sep 2005 (1 yr 3 mo) | Bengaluru, India

- Contributed to Windows-based applications managing large-scale customer data in the Power Sector domain.
- Ramped on C#, .NET, XML, and ASP.NET; delivered production-quality software as a fresh graduate.

PERSONAL GITHUB PROJECTS

github.com/yajnas07

modernCpp *[C++]*
github.com/yajnas07/modernCpp
Experiments with C++11/14 features: move semantics, lambdas, variadic templates, and modern idioms.

manim *[Python]*
github.com/yajnas07/manim
Programmatic animation scripts using Manim for explaining hardware/software concepts, algorithm visualizations, and AI/EDA methodology presentations.

games / game-of-life *[JavaScript]*
github.com/yajnas07/games · yajnas07.github.io/games
Nine browser-based arcade games (Bubble Pop, Ludo, Maze, Snakes & Ladders, Tic-Tac-Toe …) in vanilla HTML/CSS/JS. Also includes Conway's Game of Life.

forKids / learnr *[C++ / HTML]*
github.com/yajnas07/forKids · yajnas07.github.io/learnr
Educational platform for children: beginner-friendly C++ programs and an interactive web portal covering Maths, Science, and Social Science for school students.

PUBLICATIONS & PATENTS

[Conference] Enabling Reset in SystemC-based Virtual Platforms — *ISCUG 2013*

[Conference] Accelerating SystemC SoC Development Using Text-Based Netlist Connectivity Specification

[Conference] Innovative Flow for Reuse of IP C Models from IVAHD 2.0 Design to Virtual Platform Simulator for Pre-Silicon Software Development

[Patent] Method and System for Emulating an Image Processing System — *Granted*

EDUCATION

M.S., Microelectronics — Birla Institute of Technology and Science (BITS), Pilani *(2009–2010)*

B.Tech., Computer Science & Engineering — National Institute of Technology (NIT), Tiruchirappalli *(2000–2004)*

INTERESTS & SIDE PROJECTS

LLM/GenAI experimentation (RAG, agentic tools, LLM + EDA) • Manim programmatic animations • Building browser-based arcade games (vanilla JS) • Educational content for children (learnr portal) • Technical blogging (codepuz.blogspot.com) • Atijeevan Foundation (volunteer — acid-attack survivor rehabilitation NGO)